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Performance Comparison of A 8X8 Array of SRAM Cells Designed Using Mtcmos and FinFET

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ABSTRACT - The down scaling of conventional CMOS has made power consumption a matter of serious concern today. The reduction in channel length results in interaction of the depletion widths of the source and drain in MOSFETs, thereby inducing faster carrier transport and hence, larger off state currents. Hence, the gate loses control on the channel. This leakage contributes significantly to static power dissipation especially when lower technology nodes are used. This motivates the need of introducing an additional gate which has improved control on the channel. One such double gate device extensively under research today is the FinFET, which is believed to be a promising candidate for replacing conventional CMOS devices to address the issue of sub-threshold leakage.

This paper comprises of a detailed study of various SRAM parameters such as leakage current, total average power consumption, and delay. The parameters were studied for a single cell, the sram cell was designed using conventional 6T structure using Mosfet in 45nm technology, low power technique used for improvement was MTCMOS and finally the cell was designed using double gate device FinFET (30nm).SRAM cells find huge application in portable hand held devices. This calls for using multiple 1bit cells. Hence an array of 8X8 sram was designed and results were obtained. The performance parameters such as leakage current and power consumption shows a significant improvement when MTCMOS technique is used and a further improvement in performance parameters is seen when we use Finfet based array of SRAM cells. The performance of the device for low power applications and the leakage involved are analyzed using CADENCE tool.

Keywords - Leakage current, power consumption, delay, low power technique MTCMOS, FinFET.

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1 INTRODUCTION

An integral part of all the processors and portable devices being used today is memory arrays. These arrays constitute of several SRAM cells, these cells stores a single bit of data hence for storing a large amount of data we need a large number of SRAM cells. These cells are designed in various configuration based on the number of transistors being used.

With increasing demand for the portable devices the power consumption has become major concern in VLSI chip designing. Technology scaling has resulted in a significant increase in leakage current of CMOS devices which has increased the Power consumption of the devices. Hence in this work MTCMOS technique is used to reduce the leakage current and power consumption in 45nm technology. Moving on to the recent trend the double-gate FET has become a popular device candidate for future generations of CMOS technology The FinFET, has received a great deal of attention lately as a double-gate FET that is more amenable to conventional CMOS processing Unlike planar single- and double-gate devices, in case of FinFET effective channel width is perpendicular to the semiconductor plane.

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Therefore, it is possible to increase the effective channel width and drive current per unit planar area by increasing the fin-height. Interconnect dominated circuits such as memory arrays are likely to get benefited from the increased driving current.

The paper is organized as follows section II III and IV describes about the FinFET technology, structure and operation of conventional 6T SRAM cell and the MTCMOS technique used in SRAM cell respectively. Section V describes about the results of the designed array and finally section VI concludes the entire work.

2 FINFET TECHNOLOGY

The FinFET transistor is a vertical double-gate Device and is regarded as a promising alternative for Sub-45 nm bulk devices.

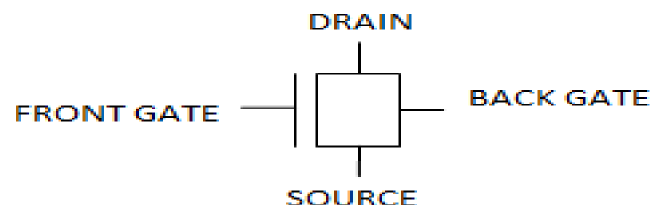

Figure1. FinFET Symbol

Figure 1 shows the symbol of a multi-fin double gate FinFET device. Current flow is parallel to the wafer plane. The thickness of the single fin is equal to the silicon channel thickness. Each fin accounts for the width of the device, and H is the height of each fin.
A unique property of the FinFET is the electrical coupling between the front and back gates. The implication of this coupling is that the threshold voltage of the front gate (Vthf) is not only established by the process, but also it can be controlled by the back gate voltage (VGb). This can be compared to the body effect in a bulk transistor [3].

An independent-gate FinFET operates in the dual gate mode (DGM) when both gates are biased to induce channel inversion. Alternatively, an independent-gate n-FinFET (p-FinFET) operates in the Single-gate mode when one of the gates is deactivated by connecting the gate to ground (VDD). If one of the gates in the single-gate mode (SGM) is disabled it increases the absolute value of the threshold voltage compared to DGM. Therefore, it is possible to modulate the threshold voltage of the FinFET by biasing the two gates independently.
The sram cell in this work is designed using the Finfet devices the drivers and the access transistors are n-type and load transistors are of p-type.

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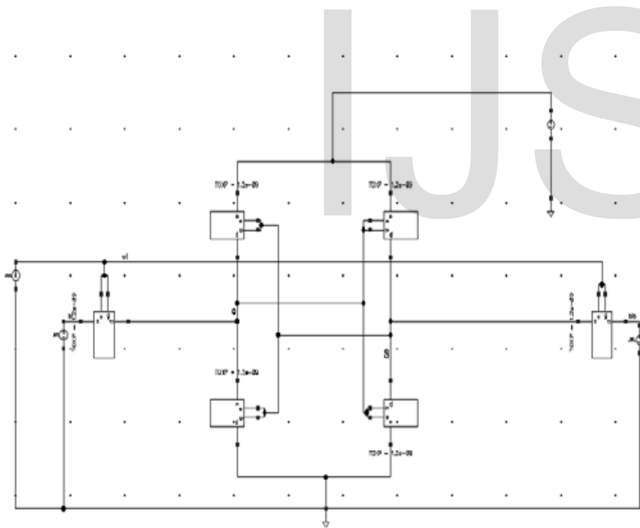

Fig2: Schematic of SRAM cell using Finfet

3 CONVENTIONAL 6T CMOS SRAM CELL

A. *Write Operation*

For a successful write, the bit cell becomes mono-stable, forcing the internal voltages to the correct values. If the cell retains bi-stability then the write operation does not occur. For write operation, the WL is activated and bit-lines are connected to ground or Vdd depending upon write-0 or 1 operation. During write-l operation, BL is connected to Vdd but, stored node 'Q' does not reach to Vdd owing to voltage dividing effect across the access transistor and drive transistor node, which degrades the writability. Similarly, for write-0 operation same problem occurs.

B. *Read Operation*

For a successful Read operation, the bit cell becomes bi-stable, forcing to retain the internal voltages to the correct values If the Cell retains bi-stability then only the read operation occurs properly. In conventional 6T SRAM cell, for read operation, the bit-lines are pre-charged to supply voltage (Vdd) and then word line (WL) is activated. The internal node of the bit cell, representing zero, gets pulled upward through the access transistor. This is due to the voltage dividing effect across the access transistor and drive transistor.

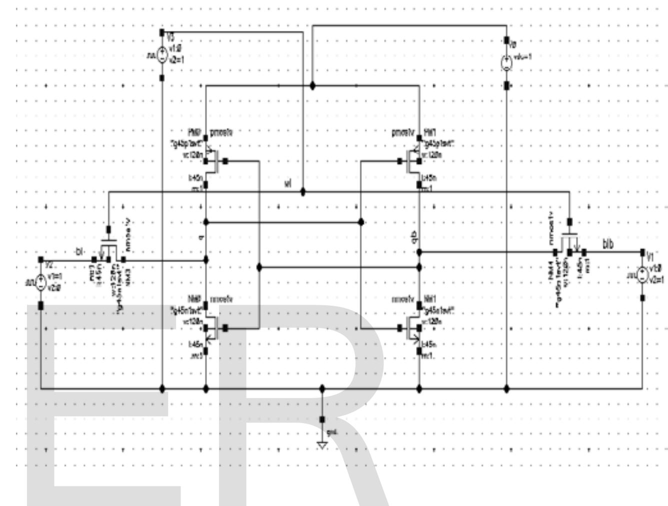

Fig3: Schematic of 6T SRAM cell

4 MTCMOS TECHNIQUE

In MTCMOS technique, here we have low VTCMOS circuit present, and we are adding two additional transistors known as sleep transistors. So, one p MOS and one n MOS transistors are added in series with the designed circuit. In MTCMOS technique we essentially design our logic circuit using transistors with low Vth value the access transistor , the driver transistor and the load transistor all are designed using low Vth. Now we add pmos and nmos in series with this circuit where the series transistors are high Vth transistors. The pmos is connected to Vdd and nmos is connected to ground and then we apply sleep signals to these high Vth transistors. A sleep signal is used and this is connected t input of the high Vth transistors through an inverter also designed using high Vth so that they get complementary inputs. This means when circuit is in normal mode of operation both these transistors are on and these transistors are essentially high Vth transistors. So, the current that will be passing through it will be dependent on the current of this particular circuit, because both the transistors are on, and if the input is say 0 volt, then the leakage current will be dependent on the leakage current of this transistor. So, in the normal mode of operation, the

current that will be flowing will correspond to the low V t transistors and these points we will act as kind of virtual Vdd and virtual ground.

Now in the active mode we make these transistors off that mean we apply a value of 1 to the sleep signal. So, when we do that, then pmos transistor and nmos transistor, both are now off. So, when both of them are off, there are no longer virtual ground and virtual Vdd points. We may say that, now the high Vth transistors are series with low Vth transistors.

So, current will be dependent on the lower of the two, because they are in series, when two currents are in series, we know that lower current will flow through, as the high V t transistors are having lower leakage current, smaller current leakage current will flow. So, this is the basic idea behind this MTCMOS.

So, in MTCMOS circuit, we are having both high Vth and low Vth transistors, and the design flow is more or less similar, except that we will be adding two transistors in series. The leakage current will be reduced, because the high Vth transistors in series with the low Vth transistors, and we get smaller leakage power in the standby mode.

$$Vt \downarrow = DELAY \downarrow + I\ leakage \uparrow$$

Low - threshold voltage (Vth) provides high performance.

$$Vt \uparrow = DELAY \uparrow + I\ leakage \downarrow$$

High - threshold voltage (Vth) reduces sub threshold leakage.

5 Results and Discussion

A. Delay Calculation:

Write operation of the designed SRAM arrays were studied for finding the delay in a successful write operation fig 4, fig 5 and fig 6 respectively shows the write operation of an array designed using CMOS MTCMOS and FinFET technologies.

When cells are used in array we need a row decoder circuit which selects the row of access transistor. The word line associated with the entire row goes high which turns the access transistor on, and then depending on the selected bit line a particular cell from an array is selected. We see here that when word line goes high depending on the input provided by the bit line and the previously

Stored values at the output node Q and QB a write operation is performed.

a) Write "1" operation: A write 1 operation takes place when we set the bit line high and bit line bar to a low logic level using appropriate pulse signals and a value of 0 is stored at the output node Q and 1 at the output node QB. This is illustrated in the waveforms.

b) Write "0" operation: A write 0 operation takes place when we set the bit line low and bit line bar to a high logic level using appropriate pulse signals and a value of 1 is stored at the output node Q and 0 at the output node QB. This is illustrated in the waveform

c) Read "1" operation: A pre-charge circuit is used to charge the bit lines to logic level high and a 1 is stored at the output node Q. with the help of a pre-charge circuitry the bit lines are charged high and when the word line goes high the access transistors are on causing bit line bar to discharge at this instant of time the bit line takes a value slightly higher than 1 and this ensures the output 1 stored at the node Q of the SRAM is successfully read and hence we get a successful read 1 operation.

d) Read "0" operation: A pre-charge circuit is used to charge the bit lines to logic level high and a 0 is stored at the output node Q. with the help of a pre-charge circuitry the bit lines are charged high and when the word line goes high the access transistors are on causing bit line to discharge at this instant of time the bit line takes a value approximately 1and this ensures the output 0 stored at the node Q of the SRAM is successfully read and hence we get a successful read 0 operation.

In an array we need an additional circuitry of sense amplifier associated with each column. The bit line and bit line bar is fed as the input and the amplifier senses the difference in the value and then amplifies the value. The basic differential voltage mode sense amplifier is used in this work.

The output shown is of arrays which shows both the write 1 and write 0 operations successfully being carried out.

An additional sleep signal is used to control the sleep transistors in MTCMOS as shown in fig 5. When the sleep signal is low implying that both the high Vth sleep transistors are in such a scenario the sram cell performs the normal write operations. When the sleep signal goes high the sleep transistors are no more active and hence the sram cells retain the initially stored values.

TABLE 1

DELAY COMPARISION

TYPE OF SRAM ARRAY	DELAY in (picoseconds)
CMOS	19.38
MTCMOS	20.03
FinFET	1.30

We can see from the table that delay in case of MTCMOS is slightly more because of the high Vth transistors used and in case of Finfet the delay is least.

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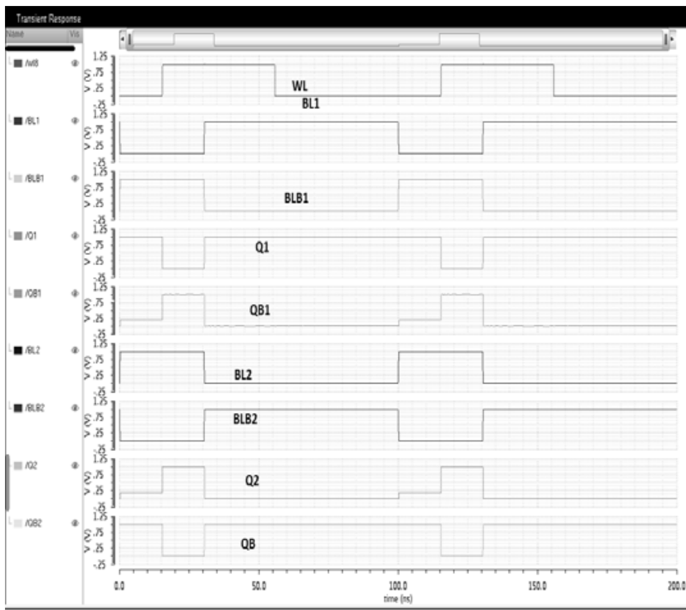

Fig 4: write operation of CMOS array

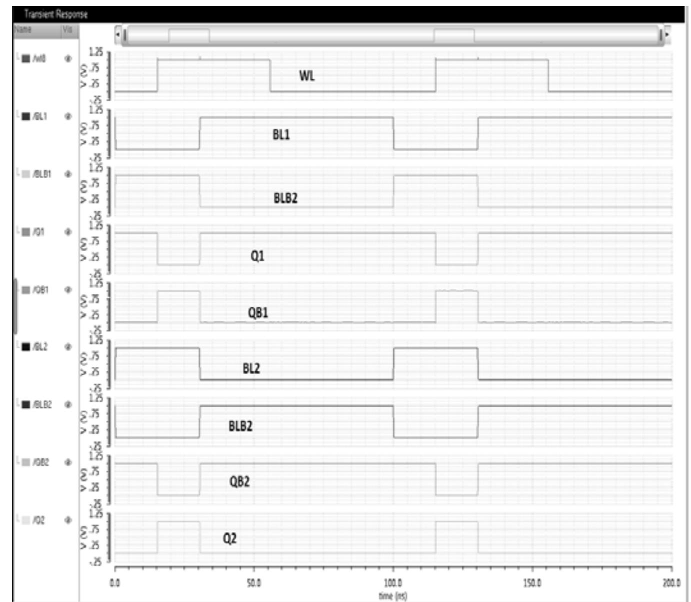

Fig 6: write operation of FinFET array

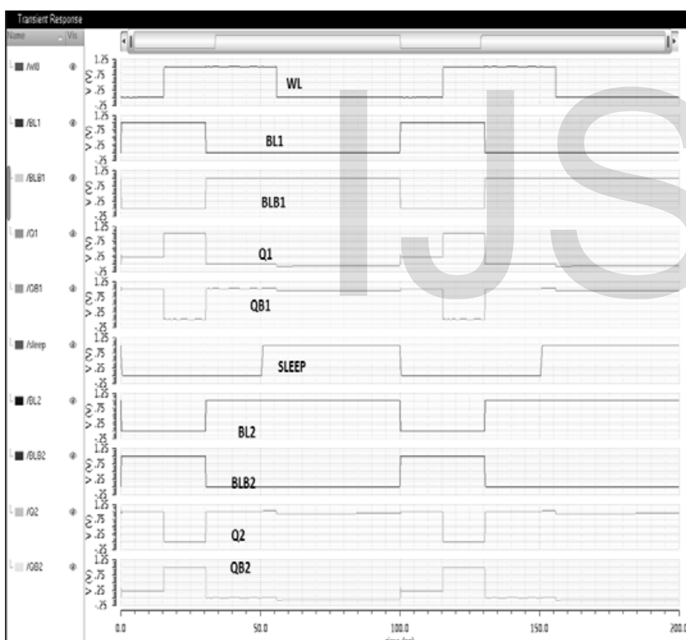

Fig5: write operation of MTCMOS array

B. LEAKAGE CURRENT:

Leakage current is the unintended loss of electrical current or electrons. Leakage is in fact, a problem that inhibits the faster advancements in performance. Semiconductors make use of millions of transistors to perform calculations and store data. Leakage current in semiconductors occurs at the transistor level.

As semiconductor manufacturers continue to make transistors smaller to squeeze more onto a chip, problems with leakage increase. Smaller transistors have thinner insulating layers, causing more leakage current. As we are scaling down the technology the leakage current is of prime concern due to the short channel effects the contribution of this current towards the total power increases.

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When the transistor is not turned on there should be no current flowing ideally. But even in the off state there's a current flow in the device this current is termed as sub-threshold leakage current. The threshold voltage and the leakage current have an inverse relation between them.

Apart from sub threshold leakage current, gate leakage, and tunneling current also constitute in the total leakage current. Leakage in transistors causes SRAM to require more power to operate, as they must replace the current lost due to leakage. The leakage current generates heat as it leaks away, which leads to degraded performance for the SRAM. When the heat from leakage is combined with the heat generated by the SRAM normal operation, it can become a significant problem. Excessive heat can eventually cause circuit failure. There are different approaches to reduce the amount of leakage. In this work MTCMOS technique is used to reduce leakage power, the low Vth transistors that contribute for higher leakage are on only when there's a need of logical operation. And the high Vth transistor in the off state reduces a significant amount of leakage in the entire cell.

In case of double gate devices we don't need any additional method to control the leakage. The presence of double gate provides for a wider channel area and takes care for reduction of leakage current.

TABLE 2

LEAKAGE CURRENT COMPARISON

SRAM CELL	LEAKAGE CURRENT in (μA)
CMOS	25.31
MTCMOS	14.66
FinFET	8.05

C. Total Power Consumption

Owing to the application of SRAM cells in hand held devices this parameter is very crucial in choosing the right SRAM cell for an array design. The less the power consumed by the cell the better longevity or less drained is the battery of the devices in which we are using this SRAM cell based array.

Power consumption of an SRAM can be categorized into two components: switching power, also known as dynamic power, and leakage power known as static power. For power analysis the different arrays designed using all CMOS, MTCMOS and FinFET are employed. In this analysis, we will focus on the power consumed by the array because the effect of an optimal device selection on the power of SRAM peripheral circuits is insignificant compared to that on SRAM arrays.

Therefore, peripheral circuits such as decoders and sense amplifiers for read and write operations, are excluded in this power analysis. The table below contains the value of the power consumed by an 8X8 array with and without a low power technique along with the value obtained when the bulk devices are replaced with a double gate device.

TABLE 3

POWER CONSUMPTION COMPARISION

ARRAY OF SRAM CELL	TOTAL POWER CONSUMPTION in (μW)
CMOS	642.4
MTCMOS	188.7
FinFET	3.04

6 CONCLUSION

The performance of a CMOS based array is significantly improved by the use of low power technique. The MTCMOS technique applied to the CMOS based SRAM cell reduces the leakage current by *43.4 %* and power consumption by *70.62 %* the only trade off for using MTCMOS technique is the delay in the cell operations is increased which is inevitable because of the high Vth sleep transistors.

The alternative to an improved SRAM cell using MTCMOS technique is the use of FinFET. The FinFET being a double gate device is capable of reducing the leakage current and power consumption at the same time it overcomes the delay issue in MTCMOS. Hence a Finfet based SRAM cell which further improves the performance parameter significantly of the CMOS and MTCMOS based design proves to be an overall superior device of choice for a SRAM cell and array. The only factor that imposes a challenge to FinFET as an alternative is the cost of production, but considering the recent trends in technological development the FinFET is an ideally suited device for an ever increasing demand of efficiently performing systems which are needed to be fast and more compact.

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